FAST TURBO-CODE ENCODER

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention generally relates to an encoder, and more particularly, to a fast turbo-code encoder. The advantage of the encoder is the encoding data is output via less exclusive-or (XOR) gate operations. Thus, saves about half of the operation time of the conventional structure.

Description of Related Art

[0002] The error control coding is widely used in the communication system and the computer media storage. Berrou, Glavieux, and Thitimajshima first proposed the turbo-code which error-correcting capability nears to the Shannon limited error-correcting in 1993 (C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limited Error-correcting Coding and Decoding: Turbo-codes (1)," in Proc. ICC'93, May, 1993). The structures of the turbo-code encoding and decoding are shown in FIG. 1 and FIG. 2. Wherein, the encoding structure comprises two recursive systematic convolution encoder (hereafter abbreviated as RSC). The characteristic of the RSC is encoding two convolution codes having the same structure together, thus the receiving end is able to decode the message repeatedly. Since the characteristic of the repeatedly decoding, thus provides the excellent error-correcting capability. And since the excellence of the error-correcting capability, the turbo-codes are widely applied in the communication system. For example, like applied in the CDMA transmission system (J. Blaanz, P. Jung, and M. Na B han, "Realistic Simulations of CDMA Mobile Radio Systems Using Joint Detection

and Coherent Receiver Antenna Diversity," IEEE third International Symposium on Spread Spectrum Techniques and Applications, Oulu Finland, 1994).

[0003] When Berrou and Benedetto proposed the turbo-codes encoding structure, the RSC and the non-recursive systematic convolution (NSC) is compared. In most of the communication conditions, the RSC has larger minimum distance of the codes and the better error-correcting efficiency. Thus, two RSC are parallelized to form a turbo-code operation structure. Whereas, since the recursive characteristic of the RSC, the encoding process has a longer time delay, this is an existing disadvantage of using the turbo-codes.

SUMMARY OF THE INVENTION

[0004] To solve the problem mentioned above, the present invention provides a fast turbo-code decoder. The advantage of the encoder is the encoding data is output via less exclusive-or (XOR) gate operations. Thus, saves half of the operation time comparing to the conventional structure.

[0005] To achieve the objective mentioned above, the present invention provides a turbo-code fast encoding device that is suitable for the communication system. The device is suitable for outputting a parity information after the encoding process on a turbo-code of the sequential input. Wherein, the input bit sequence of the turbo-code is represented as $d=(d_1,d_2,\ldots,d_k,\ldots,d_N)$, where the d_k is the input bit of the turbo-code fast encoding device at time k, k is from 1 to N, and N is the segment length. Wherein, the turbo-code fast encoding device comprises a first recursive systematic convolution (RSC) encoder and a second recursive systematic convolution (RSC) encoder. The first recursive systematic convolution (RSC) encoder and the second recursive systematic convolution (RSC) encoder all have

$$y_k = d_k + \sum_{i=1}^{M} g_{di} a_{k-i}$$

Wherein, d_k is the input bit of the turbo-code fast encoding device at time k, y_k is the parity information corresponding to d_k, g_{di} is the parameter that is generated by a first encoder feed-forward generator, the element is either 0 or 1, whereas, a_{k-i} is generated by *i*th register at time k.

[0006] The turbo-code fast encoding device mentioned above, wherein, the output of the first encoder at time k is represented as $C_K=(X_k,Y_{1K})$. Because the encoder is systematic, so $X_k=d_k$. A parity output is represented as $Y_{1k} = \sum_{i=0}^{M} g_{1fi} a_{k-i}$, herein, M is the memory order of the encoder, $(g_{1f1}, g_{1f2}, \dots g_{1fM})$ is defined such like G_{1f} is the first encoder feed-forward generator, the element is either 0 or 1.

[0007] The turbo-code fast encoding device mentioned above, wherein, the following equation $a_k = d_k + \sum_{i=1}^{M} g_{1bi} a_{k-i}$ can be obtained from the first encoder. With the same reason, $(g_{1bf1}, g_{1b2}, \dots g_{1bM})=G_{1b}$ is called as the first encoder feedback generator, thus the following general equation is obtained:

$$y_{1k} = \sum_{i=0}^{M} g_{1fi} a_{k-i} = a_k + \sum_{i=1}^{M} g_{1fi} a_{k-i} = (d_k + \sum_{i=1}^{M} g_{ibi} a_{k-i}) + \sum_{i=1}^{M} g_{1fi} a_{k-i}$$

the above equation can be re-arranged as follows:

$$y_{1k} = d_k + \sum_{i=1}^{M} (g_{1bi} + g_{1fi}) a_{k-i} \equiv d_k + \sum_{i=1}^{M} g_{1di} a_{k-i}$$

[0008] The turbo-code fast encoding device mentioned above, wherein, the $G_{1d} = 1 \| \sum_{i=1}^{M} g_{1di} = 1 \| \sum_{i=1}^{M} (g_{1bi} + g_{1fi})$ is defined and called as the parameter of the first

encoder direct-feed-forward generator, where the || represents two rows of the binary numbers that are serially concatenated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention. In the drawings,

[0010] FIG. 1 schematically shows a turbo-code encoder comprising of two parallel RSC encoders;

[0011] FIG. 2 schematically shows the decoding structure of the turbo-code;

[0012] FIG. 3 schematically shows a structure of a fast RSC encoder;

[0013] FIG. 4 schematically shows a conventional structure of a fast RSC encoder, wherein G_f=1101, G_b=1011; and

[0014] FIG. 5 schematically shows a structure of a fast RSC encoder of a preferred embodiment of the invention, wherein G_f=1101, G_d=1110.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] A turbo-code encoder comprises two parallel RSC encoders (RSC 1 and RSC 2 as shown in FIG. 1), the sequence of the input bit is represented as $d=(d_1,d_2,\ldots,d_k,\ldots,d_N)$, where the d_k is the input bit of the encoder at time k, k is from 1 to N, and N is the segment length. The output of the first encoder RSC 1 at time k is represented as $C_K=(X_k,Y_{1K})$. Because the encoder is systematic, so $X_k=d_k$. Another

parity output is represented as $Y_{1k} = \sum_{i=0}^{M} g_{1fi} a_{k-i}$, herein, M is the memory order of the encoder, $(g_{1f1}, g_{1f2}, \ldots g_{1fM})$ is defined as G_{1f} is the first encoder feed-forward generator, the element is either 0 or 1. The first encoder is also called as the RSC 1 encoder. The following equation $a_k = d_k + \sum_{i=1}^{M} g_{1bi} a_{k-i}$ can be obtained from the encoder. With the same reason, $(g_{1bf1}, g_{1b2}, \ldots g_{1bM}) = G_{1b}$ is called as the first encoder feedback generator, thus the following general equation is obtained:

$$y_{1k} = \sum_{i=0}^{M} g_{1fi} a_{k-i} = a_k + \sum_{i=1}^{M} g_{1fi} a_{k-i} = (d_k + \sum_{i=1}^{M} g_{ibi} a_{k-i}) + \sum_{i=1}^{M} g_{1fi} a_{k-i} \tag{1}$$

the above equation can be re-arranged as follows:

$$y_{1k} = d_k + \sum_{i=1}^{M} (g_{1bi} + g_{1fi}) a_{k-i} \equiv d_k + \sum_{i=1}^{M} g_{1di} a_{k-i} \tag{2}$$

[0016] The structure of the fast RSC encoder designed based on this is shown in FIG. 3. Herein, defines

$$G_{1d} = 1 \| \sum_{i=1}^{M} g_{1di} = 1 \| \sum_{i=1}^{M} (g_{1bi} + g_{1fi}) \tag{3}$$

called as the parameter of the first encoder direct-feed-forward generator, wherein, the || represents two rows of the binary numbers are serially concatenated, for example, 1 || 001=1001. With the same reason, $y_{2k} = d_k + \sum_{i=1}^{M} g_{2di} a_{k-i}$, thus, can be written as the following general equation:

$$y_{hk} = d_k + \sum_{i=1}^{M} g_{hdi} a_{k-i} \tag{4}$$

[0017] Herein, the subscript h of y is either 1 or 2 that represents the number of the RSC encoder. The structure of the RSC encoder 1 and the RSC encoder 2 are the same in

current turbo-code application. Thus, the number h is omitted, obtains $y_k = d_k + \sum_{i=1}^{M} g_{di} a_{k-i}$, the circuit diagram of the RSC encoder based on this design is shown in FIG. 3.

[0018] For easy to describe, the turbo-code of the third generation CDMA mobile communication standard is exemplified here as a preferred embodiment according to the present invention. The quantity of the register of the RSC encoder M=3, whereas, the RSC encoder 2 is the same as the RSC encoder 1, so $g_{1bi}=g_{2bi} \quad g_{bi}$ and $g_{1fi}=g_{2fi} \quad g_{bi}$, where the code ratio R=1/3, as shown in FIG. 4, the parameters of the feedback generator and the feed-forward generator are G_f=1101, G_b=1011 respectively. The equation is represented as follows:

$$
\begin{aligned}
y_k &= d_k + \sum_{i=1}^{M} g_{fi} a_{k-i} = a_k + a_{k-1} + a_{k-3} = (d_k + a_{k-2} + a_{k-3}) + a_{k-1} + a_{k-3} \\
&= d_k + a_{k-1} + a_{k-2} = 1d_k + 1a_{k-1} + 1a_{k-2} + 0a_{k-3}
\end{aligned}
\qquad (5)
$$

[0019] From equation (5) and based on the definition of equation (3), the parameter of the direct-feed-forward generator is obtained as G_d=1110, thus, the RSC encoder can be simplified as shown in FIG. 5. From equation (2), the encoding structure only uses only half of the exclusive-or (XOR) gate operations comparing to the conventional encoder to encode one bit. Comparing FIG. 4 and FIG. 5, the encoder of FIG. 4 needs via four exclusive-or gate operations to encode one bit, whereas, the encoder of the FIG. 5 only needs via two exclusive-or gate operations to encode one bit, thus, the speed is double.

[0020] The present invention provides a fast turbo-code encoding method and device. Wherein, the new structure of the encoder directly processes the exclusive-or operation on the input data and the internal value of the register. Thus, the encoding output is

obtained via less exclusive-or gate time. As shown in equation (2), saves about half of the operation time of the conventional structure.

[0021] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.